locking sectors which have no unerased cells; and

repeating the applying and locking steps until all sectors are locked.

B1 Contd

91. The method of claim 90, wherein said unlocking step includes setting an erase enable latch associated with individual sectors, and wherein said locking step includes resetting the latch associated with individual sectors.

92. The method of claim 90, wherein said erasure pulse is simultaneously applied to all of said sectors.

93. An erasure circuit for erasing a non-volatile electronically erasable and programmable integrated circuit memory, comprising:

erasure pulse means for selectively applying an erasure pulse to sectors of said memory;

erasure determining means for determining if each cell of a sector has been erased until an unerased cell is found; and

locking means connected to the erasure determining means for locking a sector if all cells of said sector are erased.

94. The erasure circuit of claim 93, further comprising:

means for dividing said sectors into groups; and

group application means for simultaneously applying said erasure pulse to all of the sectors in a group.

95. The erasure circuit of claim 93, wherein said erasure pulse means includes a latch associated with individual sectors, and wherein said locking means includes a control circuit for setting and resetting said latches.

96. A circuit for locking a sector in a non-volatile electrically erasable and programmable integrated circuit memory that is divided into N sectors selected separately by addressing circuits, the cells of each sector being selected by circuits for addressing by rows and columns, the erasure of the memory being obtained by the simultaneous application of an erasure pulse to a selected combination of sectors, wherein said circuit comprises:

a gate circuit on a circuit for supplying the erasure pulse to the sector; and